Your search matched **7** of **950522** documents.

A maximum of **7** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((jtag and protocol) and ((1950 <in> py) or (1951 <in> p Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Real-time on-board bus testing**
Floyd, J.A.; Perry, M.;
VLSI Test Symposium, 1995. Proceedings., 13th IEEE , 30 April-3 May 1995
Page(s): 140 -145

[Abstract] [PDF Full-Text (400 KB)] **IEEE CNF**

2 **An integrated 16-channel CMOS time to digital converter**
Ljuslin, C.; Christiansen, J.; Marchioro, A.; Klingsheim, O.;
Nuclear Science, IEEE Transactions on , Volume: 41 Issue: 4 , Aug 1994
Page(s): 1104 -1108

[Abstract] [PDF Full-Text (352 KB)] **IEEE JNL**

3 **A vertically integrated test methodology based on JTAG IEEE 1149.1 Standard Interface**
Ruparel, K.N.; Chin, C.; Fitzgerald, J.;
ASIC Conference and Exhibit, 1991. Proceedings., Fourth Annual IEEE International , 23-27 Sept. 1991
Page(s): P11 -4/1-4

[Abstract] [PDF Full-Text (376 KB)] **IEEE CNF**

4 **Functional test and diagnosis: a proposed JTAG sample mode scan tester**
Lefebvre, M.E.;
Test Conference, 1990. Proceedings., International , 10-14 Sept. 1990
Page(s): 294 -303

[Abstract] [PDF Full-Text (592 KB)] **IEEE CNF**

5 **Tradeoff decisions made for a P1149.1 controller design [ATE]**
Vining, S.;
Test Conference, 1989. Proceedings. 'Meeting the Tests of Time'., International , 29-31 Aug. 1989
Page(s): 47 -54

[Abstract] [PDF Full-Text (444 KB)] **IEEE CNF**

6 **BIST and boundary-scan for board level test: test program pseudocode**
Tulloss, R.E.; Yau, C.W.;
European Test Conference, 1989., Proceedings of the 1st , 12-14 April 1989
Page(s): 106 -111

[Abstract] [PDF Full-Text (500 KB)] **IEEE CNF**

---

7 **IEEE-1149.1 use in design for verification and testability at Texas Instruments**
Cron, A.D.;
ASIC Seminar and Exhibit, 1989. Proceedings., Second Annual IEEE , 25-28 Sept. 1989
Page(s): P4 -1/1-5

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Your search matched **4** of **950522** documents.

A maximum of **4** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((jtag and switch) and ((1950 <in> py) or (1951 <in> py)) Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **ICEBERG: an embedded in-circuit emulator synthesizer for microcontrollers**
Ing-Jer Huang; Tai-An Lu;
Design Automation Conference, 1999. Proceedings. 36th , 21-25 June 1999
Page(s): 580 -585

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

2 **A method for synchronizing IEEE 1149.1 test access port for chip level testability access**
Bhavsar, D.;
VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on , 4-7 Jan. 1998
Page(s): 289 -292

[Abstract] [PDF Full-Text (360 KB)] **IEEE CNF**

3 **System level boundary scan in a highly integrated switch**
Hughes, W.J.;
Test Conference, 1997. Proceedings., International , 1-6 Nov. 1997
Page(s): 636 -639

[Abstract] [PDF Full-Text (432 KB)] **IEEE CNF**

4 **Experience of designing JTAG ASICS within System X**
Borland, A.;
Application and Development of the Boundary-Scan Standard, IEE Colloquium on , 19 Dec 1990
Page(s): 5/1 -5/3

[Abstract] [PDF Full-Text (128 KB)] **IEE CNF**

Your search matched **2** of **950522** documents.

A maximum of **2** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((jtag and load) and ((1950 <in> py) or (1951 <in> py) o Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A 200 MHz 2.5 V 4 W superscalar RISC microprocessor**
Sanchez, H.; Eisen, L.; Croxton, C.; Piejko, A.; Nicoletta, C.; Vo, I.; Branson, B.; Wen Wang; Quan Nguyen; Buti, T.; Hsu, L.; Saccamango, M.J.; Ratanaphanyara, S.; Philip, R.; Alvarez, J.; Weitzel, S.; Gerosa, G.;
Solid-State Circuits Conference, 1996. Digest of Technical Papers. 43rd ISSCC., 1996 IEEE International , 8-10 Feb. 1996
Page(s): 218 -219, 448

[Abstract] [PDF Full-Text (1264 KB)] **IEEE CNF**

2 **A 100 K gate sub-micron BiCMOS gate array**
Gallia, J.; Yee, A.; Wang, I.; Chau, K.; Davis, H.; Swamy, S.; Sridhar, T.; Nguyen, V.; Ruparel, K.; Moore, K.; Lemonds, C.; Chae, B.; Eyres, P.; Yoshino, T.; Pozadzides, J.; Rine, R.; Shah, A.;
Custom Integrated Circuits Conference, 1989., Proceedings of the IEEE 1989 , 15-18 May 1989
Page(s): 8.6/1 -8.6/4

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

Your search matched **2** of **950522** documents.

A maximum of **2** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((jtag and format) and ((1950 <in> py) or (1951 <in> py)) Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Design and implementation of the "G2" PowerPC™ 603e-embedded microprocessor core**
Hunter, C.; Gaither, J.;
Test Conference, 1998. Proceedings. International , 18-23 Oct. 1998
Page(s): 473 -479

[Abstract] [PDF Full-Text (700 KB)] **IEEE CNF**

2 **Semiconductor perspective on test standards**
Fleming, P.;
Test Conference, 1988. Proceedings. 'New Frontiers in Testing'., International , 12-14 Sept. 1988
Page(s): 197 -198

[Abstract] [PDF Full-Text (152 KB)] **IEEE CNF**

Your search matched **12** of **950522** documents.

A maximum of **12** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((uart) and ((1950 <in> py) or (1951 <in> py) or (1952 < Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A reusable microcontroller core's design**
Janiszewki, I.; Baraniecki, R.; Siekierska, K.;
Fall VIUF Workshop, 1999. , 4-6 Oct. 1999
Page(s): 14 -19

[Abstract] [PDF Full-Text (636 KB)] **IEEE CNF**

2 **IFIS: an online test methodology**
Yeandel, J.; Thulborn, D.; Jones, S.;
Circuits, Devices and Systems, IEE Proceedings- , Volume: 145 Issue: 1 , Feb. 1998
Page(s): 1 -6

[Abstract] [PDF Full-Text (632 KB)] **IEE JNL**

3 **An on-line testable UART implemented using IFIS**
Yeandel, J.; Thulborn, D.; Jones, S.;
VLSI Test Symposium, 1997., 15th IEEE , 27 April-1 May 1997
Page(s): 344 -349

[Abstract] [PDF Full-Text (524 KB)] **IEEE CNF**

4 **A 4*2.5 Mchip/s direct sequence spread spectrum receiver with digital IF and integrated ARM6 core**
Gyselinckx, B.; Rynders, L.; Engels, M.; Bolsens, I.;
Custom Integrated Circuits Conference, 1997., Proceedings of the IEEE 1997 , 5-8 May 1997
Page(s): 461 -464

[Abstract] [PDF Full-Text (424 KB)] **IEEE CNF**

5 **ARM7100-a high-integration, low-power microcontroller for PDA applications**
Budd, G.; Milne, G.;
Compcon '96. 'Technologies for the Information Superhighway' Digest of Papers , 25-28 Feb. 1996
Page(s): 182 -187

[Abstract] [PDF Full-Text (508 KB)] **IEEE CNF**

6 **Embedded processor applications for SONET telecommunication systems**
Bush, D.;
WESCON/'95. Conference record. 'Microelectronics Communications Technology Producing Quality Products Mobile and Portable Power Emerging Technologies' , 7-9 Nov. 1995
Page(s): 377

[Abstract] [PDF Full-Text (384 KB)] **IEEE CNF**

---

7 **Rapid migration to VLSI**
Lowinski, W.B.; Kirwan, R.; Perry, A.; Yu, T.;
Aerospace and Electronics Conference, 1992. NAECON 1992., Proceedings of the IEEE 1992 National , 18-22 May 1992
Page(s): 97 -100 vol.1

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

---

8 **Rapid migration to VLSI**
Lowinski, W.B.; Kirwan, R.; Perry, A.; Yu, T.;
Aerospace and Electronic Systems Magazine, IEEE , Volume: 7 Issue: 9 , Sept. 1992
Page(s): 21 -23

[Abstract] [PDF Full-Text (216 KB)] **IEEE JNL**

---

9 **Sendfax a single chip fax and data modem**
Lindsay, G.;
Circuits and Devices for Data Communications, IEE Colloquium on , 28 Nov 1989
Page(s): 3/1 -3/5

[Abstract] [PDF Full-Text (200 KB)] **IEE CNF**

---

10 **A single-chip 300 baud FSK modem**
Takla, A.K.; Haque, V.A.;
Solid-State Circuits, IEEE Journal of , Volume: 19 Issue: 6 , Dec 1984
Page(s): 846 -854

[Abstract] [PDF Full-Text (920 KB)] **IEEE JNL**

---

11 **MTEC: A Microprocessor System for Astronomical Telescope and Instrument Control**
Ellis, M.J.; Hovey, G.R.; Stapinski, T.E.;
Solid-State Circuits, IEEE Journal of , Volume: 15 Issue: 1 , Feb 1980
Page(s): 144 -147

[Abstract] [PDF Full-Text (584 KB)] **IEEE JNL**

---

12 **Development of an electronic control system for remote controlled underwater vehicles**
Tierney, J.; Walrod, R.;
OCEANS , Volume: 9 , Sep 1977
Page(s): 119 -124

[Abstract] [PDF Full-Text (664 KB)] **IEEE CNF**

Your search matched **19** of **950522** documents.

A maximum of **19** results are displayed, **50** to a page, sorted by **publication year** in **descending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again**.

((delimiter) and ((1950 <in> py) or (1951 <in> py) or (19 Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **A method for street number matching in Japanese address recognition**
Ogata, H.; Ueda, Y.; Marukawa, K.; Sako, H.; Fujisawa, H.;
Document Analysis and Recognition, 1999. ICDAR '99. Proceedings of the Fifth International Conference on , 20-22 Sept. 1999
Page(s): 321 -324

[Abstract] [PDF Full-Text (64 KB)] **IEEE CNF**

2 **Design consideration for multi-lingual cascading text compressors**
Chi, C.-H.; Zhang, Y.;
Data Compression Conference, 1999. Proceedings. DCC '99 , 29-31 March 1999
Page(s): 520

[Abstract] [PDF Full-Text (144 KB)] **IEEE CNF**

3 **Information technology - telecommunications and information exchange between systems - local and metropolitan area networks - specific requirements. Part 5: token ring access method and physical layer specifications**
ISO/IEC 8802-5, ANSI/IEEE Std 802.5, 3rd edn. 1998 , 26 May 1998

[Abstract] [PDF Full-Text (12500 KB)] **IEEE STD**

4 **Feature-based Thai unknown word boundary identification using Winnow**
Charoenpornsawat, P.; Kijsirikul, B.; Meknavin, S.;
Circuits and Systems, 1998. IEEE APCCAS 1998. The 1998 IEEE Asia-Pacific Conference on , 24-27 Nov. 1998
Page(s): 547 -550

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

5 **Fault-tolerant broadcasts in CAN**
Rufino, J.; Verissimo, P.; Arroz, G.; Almeida, C.; Rodrigues, L.;
Fault-Tolerant Computing, 1998. Digest of Papers. Twenty-Eighth Annual International Symposium on , 23-25 June 1998
Page(s): 150 -159

[Abstract] [PDF Full-Text (272 KB)] **IEEE CNF**

6 **A system for segmentation and recognition of totally unconstrained handwritten numeral strings**
Shi, Z.; Srihari, S.N.; Shiu, Y.-C.; Ramanaprasad, V.;
Document Analysis and Recognition, 1997., Proceedings of the Fourth International Conference on , Volume: 2 , 18-20 Aug. 1997
Page(s): 455 -458 vol.2

[Abstract] [PDF Full-Text (380 KB)] **IEEE CNF**

---

7 **Information technology - telecommunications and information exchange between systems - local and metropolitan area networks - specific requirements. Part 5: token ring access method and physical layer specifications**
ISO/IEC Std 8802-5, 1995, ANSI/IEEE Std 802.5-1995 , 29 Dec. 1995

[Abstract] [PDF Full-Text (12984 KB)] **IEEE STD**

---

8 **4.0 Structure Delimiter Statements**
IEEE Std 716-1995 , 12 Oct. 1995
Page(s): 9

[Abstract] [PDF Full-Text (92 KB)] **IEEE STD**

---

9 **A language for document generic layout description and its use for segmentation into regions**
Azokly, A.; Ingold, R.;
Document Analysis and Recognition, 1995., Proceedings of the Third International Conference on , Volume: 2 , 14-16 Aug. 1995
Page(s): 1123 -1126 vol.2

[Abstract] [PDF Full-Text (400 KB)] **IEEE CNF**

---

10 **Fieldbus interface control IC**
Yoshida, Y.; Mizoe, K.; Matsuda, A.; Kuroiwa, S.;
Instrumentation and Measurement Technology Conference, 1994. IMTC/94. Conference Proceedings. 10th Anniversary. Advanced Technologies in I & M., 1994 IEEE , 10-12 May 1994
Page(s): 428 -431 vol.1

[Abstract] [PDF Full-Text (200 KB)] **IEEE CNF**

---

11 **Blush and Zebrackets: large- and small-scale typographical representation of nested associativity**
Cohen, M.;
Visual Languages, 1992. Proceedings., 1992 IEEE Workshop on , 15-18 Sept. 1992
Page(s): 264 -266

[Abstract] [PDF Full-Text (296 KB)] **IEEE CNF**

---

12 **Text compression using several Huffman trees**
Basu, D.;
Data Compression Conference, 1991. DCC '91. , 8-11 April 1991
Page(s): 452

[Abstract] [PDF Full-Text (52 KB)] **IEEE CNF**

---

13 **Frame content independent stripping for token rings**

Ramakrishnan, K.K.; Yang, H.;
Local Computer Networks, 1990. Proceedings., 15th Conference on , 30 Sept.-3 Oct. 1990
Page(s): 405 -415

[Abstract] [PDF Full-Text (1172 KB)] **IEEE CNF**

---

14 **Description of and experimental results for a high data rate underwater acoustic telemetry link**
Estes, L.E.; Fain, G.; Caron, P.;
Autonomous Underwater Vehicle Technology, 1990. AUV '90., Proceedings of the (1990) Symposium on , 5-6 June 1990
Page(s): 304 -312

[Abstract] [PDF Full-Text (356 KB)] **IEEE CNF**

---

15 **Error characteristics of fiber distributed data interface (FDDI)**
Jain, R.;
Communications, IEEE Transactions on , Volume: 38 Issue: 8 , Aug. 1990
Page(s): 1244 -1252

[Abstract] [PDF Full-Text (944 KB)] **IEEE JNL**

---

16 **Access control module for local integrated optical network**
Pallios, V.; Antonakopoulos, T.; Makios, V.;
Electronics Letters , Volume: 25 Issue: 3 , 2 Feb. 1989
Page(s): 183 -185

[Abstract] [PDF Full-Text (264 KB)] **IEE JNL**

---

17 **A high speed access mechanism for a multiservice LAN at 144 Mbps**
Pallios, V.; Antonakopoulos, T.; Makios, V.;
Electrotechnics, 1988. Conference Proceedings on Area Communication, EUROCON 88., 8th European Conference on , 13-17 June 1988
Page(s): 256 -260

[Abstract] [PDF Full-Text (316 KB)] **IEEE CNF**

---

18 **On the Impact of HDLC Zero Insertion and Deletion on Link Utilization and Reliability**
Joong Ma;
Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 30 Issue: 2 , Feb 1982
Page(s): 375 -381

[Abstract] [PDF Full-Text (592 KB)] **IEEE JNL**

---

19 **The parsing program for automatic text-to-speech synthesis developed at the electrotechnical laboratory in 1968**
Umeda, N.; Teranishi, R.;
Acoustics, Speech, and Signal Processing [see also IEEE Transactions on Signal Processing], IEEE Transactions on , Volume: 23 Issue: 2 , Apr 1975
Page(s): 183 -188

[Abstract] [PDF Full-Text (704 KB)] **IEEE JNL**

Home | Log-out | Journals | Conference Proceedings | Standards | Search by Author | Basic Search | Advanced Search
Join IEEE | Web Account | New this week | OPAC Linking Information | Your Feedback | Technical Support | Email Alerting
No Robots Please | Release Notes | IEEE Online Publications | Help | FAQ| Terms | Back to Top

Search Results

Search Results for: **[(switch AND format) AND (boundary-scan OR jtag)<AND>(meta_published_date <= 03-01-1999)]**
Found **7** of **114,152 searched.**

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: Title Publication Publication Date Score Binder

Results 1 - 7 of 7 short listing

1 The network architecture of the Connection Machine CM-5 (extended abstract) 82%
Charles E. Leiserson , Zahi S. Abuhamdeh , David C. Douglas , Carl R. Feynman , Mahesh N. Ganmukhi , Jeffrey V. Hill , Daniel Hillis , Bradley C. Kuszmaul , Margaret A. St. Pierre , David S. Wells , Monica C. Wong , Shaw-Wen Yang , Robert Zak
Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures June 1992

2 System-chip test strategies 80%
Yervant Zorian
Proceedings of the 35th annual conference on Design automation conference May 1998

3 Cost effective satellite development with use of an Ada microprocessor 77%
Arne Carlsson
Proceedings of the conference on TRI-Ada '95: Ada's role in global markets: solutions for a changing complex world November 1995

4 Embedding Linux in a Commercial Product: A look at embedded systems and what it takes to build one 77%
Joel R. Williams
Linux Journal January 1999

5 Realization of a programmable parallel DSP for high performance image processing applications 77%
Jens Peter Wittenburg , Willm Hinrichs , Johannes Kneip , Martin Ohmacht , Mladen Bereković , Hanno Lieske , Helge Kloos , Peter Pirsch
Proceedings of the 35th annual conference on Design automation conference May 1998

6 Algorithms to compute bridging fault coverage of IDDQ test sets 77%
Paul Thadikaran , Sreejit Chakravarty , Janak Patel
ACM Transactions on Design Automation of Electronic Systems (TODAES) July 1997
Volume 2 Issue 3
We present two algorithms, called list-based scheme and tree-based scheme, to compute bridging fault (BF) coverage of IDDQ tests. These algorithms use the novel ideal of "indistinguishable pairs," which makes it more efficient and versatile than known fault simulation algorithms. Unlike known algorithms, the two algorithms can be used for combinational as well as sequential circuits and for arbitrary sets of BFs. Experiments sho ...

7 SIESTA: a multi-facet scan design system 77%
Sridhar Narayanan , Charles Njinda , Rajesh Gupta , Melvin Breuer
Proceedings of the conference on European Design Automation November 1992

Results 1 - 7 of 7 short listing

Search Results

Search Results for: **[(start bit AND format) AND (boundary-scan OR jtag)<AND>(meta_published_date <= 03-01-1999)]**
Found **1** of **114,152 searched.**

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: **Title** **Publication** **Publication Date** **Score** Binder

Results 1 - 1 of 1 **short listing**

1 The network architecture of the Connection Machine CM-5 (extended abstract) 77%
Charles E. Leiserson , Zahi S. Abuhamdeh , David C. Douglas , Carl R. Feynman , Mahesh N. Ganmukhi , Jeffrey V. Hill , Daniel Hillis , Bradley C. Kuszmaul , Margaret A. St. Pierre , David S. Wells , Monica C. Wong , Shaw-Wen Yang , Robert Zak
Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures June 1992

Results 1 - 1 of 1 **short listing**

Search Results

Search Results for: **[(protocol) AND (boundary-scan OR jtag)<AND>(meta_published_date <= 03-01-1999)]**
Found **16** of **114,152 searched.**

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: Title Publication Publication Date Score Binder

Results 1 - 16 of 16 short listing

1 The network architecture of the Connection Machine CM-5 (extended abstract) 91%
Charles E. Leiserson , Zahi S. Abuhamdeh , David C. Douglas , Carl R. Feynman , Mahesh N. Ganmukhi , Jeffrey V. Hill , Daniel Hillis , Bradley C. Kuszmaul , Margaret A. St. Pierre , David S. Wells , Monica C. Wong , Shaw-Wen Yang , Robert Zak
Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures June 1992

2 Design and performance of multipath MIN architectures 87%
Frederic T. Chong , Thomas F. Knight
Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures June 1992

3 METRO: a router architecture for high-performance, short-haul routing networks 82%
A. DeHon , F. Chong , M. Becker , E. Egozy , H. Minsky , S. Peretz , T. F. Knight
ACM SIGARCH Computer Architecture News , Proceedings of the 21ST annual international symposium on Computer architecture April 1994
Volume 22 Issue 2
The *Multipath Enhanced Transit Router Organization* (*METRO*) is a flexible routing architecture for high-performance, tightly-coupled, multiprocessors and routing hubs. A *METRO* router is a dilated cross-bar routing component supporting half-duplex bidirectional, pipelined, circuit-switched connections. Each *METRO* router is self-routing and supports dynamic message traffic. The routers works in conjunction with source-responsible network interfaces to achieve reliable en ...

4 The Starfire SMP interconnect 82%
Alan Charlesworth , Nicholas Aneshansley , Mark Haakmeester , Dan Drogichen , Gary Gilbert , Ricki Williams , Andrew Phelps
Proceedings of the 1997 ACM/IEEE conference on Supercomputing (CDROM) November 1997
The Starfire interconnect extends the envelope of Unix symmetric multiprocessor (SMP) systems in several dimensions. **Interconnect:** an active centerplane with four address routers and a 16x16 data crossbar provides 64 UltraSPARC processors with uniform memory access at a bandwidth of 10,667 MBps. **Flexibility:** Starfire can be dynamically reconfigured into multiple hardware-protected operating system domains. **Robustness:** Failing boards can be hot swapped without interrupting sy ...

5 BIST TPG for faults in system backplanes 82%
Chen-Huan Chiang , Sandeep K. Gupta
Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design November 1997

6 System-chip test strategies 80%
Yervant Zorian
Proceedings of the 35th annual conference on Design automation conference May 1998

7 A flat, timing-driven design system for a high-performance CMOS processor chipset 77%
J. Koehl , U. Baur , T. Ludwig , B. Kick , T. Pflueger
Proceedings of the conference on Design, automation and test in Europe February 1998
We describe the methodology used for the design of the CMOS processor chipset used in the IBM S/390 Parallel Enterprise Server - Generation 3. The majority of the logic is implemented by standard cell elements placed and routed flat, using timing-driven techniques. The result is a globally optimized solution without artificial floorplan boundaries. We will show that the density in terms of transistors per mm2 is comparable to the most advanced custom designs and that the impact of interconnect d ...

8 Metrology for analog module testing using analog testability bus 77%
Chauchin Su , Yue-Tsang Chen , Shyh-Jye Jou , Yuan-Tzu Ting
Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997
In this paper, we propose a method to generate high quality test waveform on chip to avoid the parasitic effects in an analog testability bus test environment. For the test response analysis, we derive an extraction methodology to remove the parasitic effects and obtain the intrinsic response of the CUT. The test results show that the algorithm is robust such that the intrinsic responses remain the same regardless of the small variation in the test waveforms. With the concept of intrinsic respon ...

9 Effective retrieval with distributed collections 77%
Jinxi Xu , Jamie Callan
Proceedings of the 21st annual international ACM SIGIR conference on Research and development in information retrieval August 1998

10 Fast prototyping: a system design flow for fast design, prototyping and efficient IP reuse 77%
Francois Pogodalla , Richard Hersemeule , Pierre Coulomb
Proceedings of the seventh international workshop on Hardware/software codesign March 1999

11 Retrospective: the MIT Alewife machine: architecture and performance 77%
Anant Agarwal
25 years of the international symposia on Computer architecture (selected papers) August 1998

12 A fast and low cost testing technique for core-based system-on-chip 77%
Indradeep Ghosh , Sujit Dey , Niraj K. Jha
Proceedings of the 35th annual conference on Design automation conference May 1998
This paper proposes a new methodology for testing a core-based system-on-chip (SOC), targeting the simultaneous reduction of test area overhead and test application time. Testing of embedded cores is achieved using the transparency properties of surrounding cores. At the core level, testability and transparency can be achieved by reusing existing logic inside the core, and providing different versions of the core having different area overheads and transparency latencies. At the chi ...

13 Gate-level test generation for sequential circuits 77%
Kwang-Ting Cheng
ACM Transactions on Design Automation of Electronic Systems (TODAES) October 1996
Volume 1 Issue 4
This paper discusses the gate-level automatic test pattern generation (ATPG) methods and techniques for sequential circuits. The basic concepts, examples, advantages, and limitations of representative methods are reviewed in detail. The relationship between gate-level sequential circuit ATPG and the partial scan design is also discussed.

14 A new complete diagnosis patterns for wiring interconnects 77%
Sungju Park
Proceedings of the 33rd annual conference on Design automation conference June 1996

15 High-level synthesis for testability: a survey and perspective 77%
Kenneth D. Wagner , Sujit Dey
Proceedings of the 33rd annual conference on Design automation conference June 1996

16 Design of heterogeneous ICs for mobile and personal communication systems 77%
Gert Goossens , Ivo Bolsens , Bill Lin , Francky Catthoor
1994 IEEE/ACM international conference on Computer-aided design November 1994
Mobile and personal communication systems form key market areas for the electronics industry of the nineties. Stringent requirements in terms of flexibility, performance and power dissipation, are driving the development of integrated circuits into the direction of heterogeneous single-chip solutions. New IC architectures are emerging which contain the core of a powerful programmable processor, complemented with dedicated hardware, memory and interface structures. In this tutorial we will d ...

Results 1 - 16 of 16 **short listing**

Search Results

Search Results for: **[(circuit AND format) AND (boundary-scan OR jtag)<AND>(meta_published_date <= 03-01-1999)]**
Found **10** of **114,152 searched.**

Search within Results

GO > Advanced Search > Search Help/Tips

Sort by: Title Publication Publication Date Score Binder

Results 1 - 10 of 10 short listing

1 The network architecture of the Connection Machine CM-5 (extended abstract) 82%
Charles E. Leiserson , Zahi S. Abuhamdeh , David C. Douglas , Carl R. Feynman , Mahesh N. Ganmukhi , Jeffrey V. Hill , Daniel Hillis , Bradley C. Kuszmaul , Margaret A. St. Pierre , David S. Wells , Monica C. Wong , Shaw-Wen Yang , Robert Zak
Proceedings of the fourth annual ACM symposium on Parallel algorithms and architectures June 1992

2 System-chip test strategies 80%
Yervant Zorian
Proceedings of the 35th annual conference on Design automation conference May 1998

3 An integrated design for testability and automatic test pattern generation system: An overview 77%
Erwin Trischler
21st Proceedings of the Design Automation Conference on Design automation June 1984
A general overview on an Integrated Design for Testability and Automatic Test Pattern Generation System (IDAS) is given. The major components of IDAS include: heuristic controllability/observability (C/O) analysis, prediction of testing costs, tools for evaluation, display and improvement of testability, and C/O guided automatic test pattern generator. The IDAS system includes also the logic and concurrent fault simulator CADAT. A brief description of major components with a scenario how to ...

4 Cost effective satellite development with use of an Ada microprocessor 77%
Arne Carlsson
Proceedings of the conference on TRI-Ada '95: Ada's role in global markets: solutions for a changing complex world November 1995

5 Embedding Linux in a Commercial Product: A look at embedded systems and what it takes to build one 77%
Joel R. Williams
Linux Journal January 1999

6 Design for testability in a silicon compilation environment 77%
H. S. Fung , S. Hirschhorn , R. Kulkarni
Proceedings of the 22nd ACM/IEEE conference on Design automation June 1985
This paper discusses design for testability automation within a silicon compiler environment under development at GTE Laboratories Inc. The proposed rule-based modular design for testability methodology utilizes both BIST and scan path techniques for full custom VLSI designs. An on-chip test controller may be used. Testability evaluation is performed using both controllability/observability and information theoretic methods. A testability "expert" is required which can manage th ...

7 Realization of a programmable parallel DSP for high performance image processing applications 77%
Jens Peter Wittenburg , Willm Hinrichs , Johannes Kneip , Martin Ohmacht , Mladen Berekovic , Hanno Lieske , Helge Kloos , Peter Pirsch
Proceedings of the 35th annual conference on Design automation conference May 1998

8 Algorithms to compute bridging fault coverage of IDDQ test sets 77%
Paul Thadikaran , Sreejit Chakravarty , Janak Patel

ACM Transactions on Design Automation of Electronic Systems (TODAES) July 1997
Volume 2 Issue 3

We present two algorithms, called list-based scheme and tree-based scheme, to compute bridging fault (BF) coverage of IDDQ tests. These algorithms use the novel ideal of "indistinguishable pairs," which makes it more efficient and versatile than known fault simulation algorithms. Unlike known algorithms, the two algorithms can be used for combinational as well as sequential circuits and for arbitrary sets of BFs. Experiments sho ...

9 Unifying test and diagnosis of interconnects and logic clusters in partial boundary scan boards 77%
Meryem Marzouki , Marcelo Lubaszewski , Mohamed Hedi Touati
Proceedings of the IEEE/ACM international conference on Computer-aided design November 1993

10 SIESTA: a multi-facet scan design system 77%
Sridhar Narayanan , Charles Njinda , Rajesh Gupta , Melvin Breuer
Proceedings of the conference on European Design Automation November 1992

Results 1 - 10 of 10 **short listing**

CiteSeer Find: uart, format Documents Citations

Searching for **PHRASE uart format**.
Restrict to: Header Title Order by: Citations Hubs Usage Date Try: Amazon B&N Google (RI) Google (Web) CSB DBLP
2 documents found. **Order: citations weighted by year.**

New Node Integration in TTP/A Networks - Elmenreich Haidinger Peti (Correct)
data. Data bytes are transmitted in a standard **UART format**. Each communication round is started by the
www.vmars.tuwien.ac.at/~wilfried/papers/rr-05-2001.pdf

New Node Integration for Master-Slave Fieldbus Networks - Peti (2002) (Correct)
data. Data bytes are transmitted in a standard **UART format**. Each communication round is started by the
www.vmars.tuwien.ac.at/~wilfried/papers/new_node_integration.pdf

Try your query at: Amazon Barnes & Noble Google (RI) Google (Web) CSB DBLP